SEAKR Engineering Reference Document (REF)

Procurement Specification for Printed Circuit Boards (PCB)

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REVISION/CHANGE RECORD

Rev.	Release Date	Author	Revision/Change Description	Pages
-	10/31/05		Initial Release	Pre-IFS
A	05/15/06		See E.O. 6365	Pre-IFS
B	10/30/06		See E.O.6683	Pre-IFS
C	08/20/08		See E.O.8066	Pre-IFS
D	04/07/09		See E.O.8476	Pre-IFS
E	06/11/10	S. Fiebig	See E.O.9400	All
F	10/18/11	J. Mayorga	Updates	9-11, 17, 20-21, 25-29
G	04/12/13	A. Thomason	Complete Re-write	ALL
H	08/16/13	A. Thomason	Update to Coupon requirements	10,13,18-20,22,23,30-32
J	02/26/15	S. Fiebig	- Add Taiyo PSR 4000 LDI to the list of approved LPI solder masks. - Add San-ei Kagaku PHP-900 IR-6P to the list of approved non-conductive via fills. - Change Appendix I section on Plating/coating thickness from 0.0015 inch min avg. to 0.00145 inch min avg. - Change microsection photo requirement to only vias that fail acceptance criteria.	15,18, 20
K	06/13/16	S. Fiebig	Add clarifications to sections 3.4.3 Hole Sizes and 4.1.1.1 Fabricator Qualification, General	16,17,23
L	09/29/16	S. Fiebig	Miscellaneous updates for IPC-6012D and IPC-6012DS	1,2,6,7, 14-15, 17-20, 22-25 Appendix 1-3
M	10/11/17	S. Fiebig	3.6.2 and Appendix I “B” foil cracks are not acceptable for Class 3. 3.4.5 “Minimum Copper Plating Thickness” applies to both the plated through hole and the surface.	13,15, 17, 19-20, 24, 30-31

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N	11/06/18	J. Fuhr	- Add IPC D Coupon Testing - Updated laminate materials to include Tachyon/Meg 6 - Clarify marking locations Remove cap plating requirement for buried vias	6, 8, 11-18, 20-21
P	05/01/19	S. Fiebig	3.1.2.4 A. – Allow fabricators to use their own script to create the coupon. 3.1.2.4 C. – Add requirement, “Not to exceed 190C”. 3.2.2.2 – Change requirement IPC-4101/41 to IPC-4103/17. 3.2.2.3 – Change requirement to call out IPC-4101/41 or IPC-4101/102. 3.12 – Change DPA requirement for Class 3/A and DS.	7, 9, 12-13, 16-17, 21-22
R	06/09/20	S. Fiebig	TOC – Delete Appendix III 1.1, 2.1, 3.11 – Remove GSFC-S312-P-003 3.1.2.4 – Clarify no D coupon testing for IPC-6012, Class 2 3.11 – Allow rework epoxy touchup of LPI solder mask 3.12 – Remove DPA requirement for IPC-6012, Class 3 Appendix III – Delete 3.5.4 – Remove GSFC-S312-P-003 4.1 – Remove GSFC-S312-P-003	5-17, 19-20, 22-26, 29-30
T	07/01/21	J. Shonts	General update to comply with IPC-6012, Revision E changes 1.2 – Added IPC-6012ES to Classification list 3.1.1.9.3 – Floating copper verification at DFM review Table 3-1 – Added for clarification of thermal shock parameters 3.1.2 – Test coupons per IPC-2221; Appendix B required 3.2.4.2.1 – Additional requirement for solder coating of critical features 3.4.12 – New section - Back-drilled Component Holes and Vias 3.5.4 – Clarified internal vs. external annular ring requirements and sampling	All

Rev.	Release Date	Author	Revision/Change Description	Pages
			3.6.2 – Added for differentiation of Fabricator vs. 3rd part microsection requirements 3.7.2 – Solder mask thickness verification by G-coupon microsection 3.11 – In the event of LPI rework, coupons subjected to additional thermal excursions to match PCBs 4.3 – Clarification of QCI requirements for Class 3 and IPC-6012ES product Other clarification and/or minor content changes as appropriate.	
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Rev.	Release Date	Author	Revision/Change Description	Pages
			4.5.1- Updated definition of “production lot” to include date code Appendix I- Updated IPC-6012 references Appendix III-Updated and clarified EIDP requirements	

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1 SCOPE

This specification shall be used for the procurement and fabrication of printed circuit boards (PCBs). Verification of PCBs shall be accomplished through the use of provisions defined herein. Detailed requirements, specific characteristics, and dimensions of the PCB are specified in the PCB fabrication drawing and may be supplemented by additional notes on the Purchase Order (PO). There shall be no substitutions or additional exceptions without written approval from SEAKR.

1.1 ADDITIONAL REQUIREMENTS

Specific requirement differences (exceptions and additions) between this document and IPC-6012 Class 3 are given in Appendix I.

Specific requirement differences (exceptions and additions) between this document and IPC-6012FS are given in Appendix II.

1.2 CLASSIFICATION

The required performance class for the PCB is listed on the PCB fabrication drawing, and definitions are in accordance with IPC-6012 or IPC-6013 (as applicable).

2 APPLICABLE DOCUMENTS

Documents referenced herein and applicable to this specification are provided for reference below. In the event a revision is not specified in context, then the most recent released revision shall apply.

2.1 GOVERNMENT/MILITARY SPECIFICATIONS AND STANDARDS

The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the applicable issues of these documents shall be those in effect on the date of the procurement. All other requirements shall default to Industry Standards.

- MIL-PRF-55110, General Specification for Printed Wiring Board, Rigid
- MIL-PRF-31032, General Specification for Printed Circuit Board/Printed Wiring Board
- NASA RP-1161, Evaluation of Multilayer Printed Wiring Boards by Metallographic Techniques
- AS/EN/SJAC AS9102, First Article Inspection

2.2 INDUSTRY STANDARDS

The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the applicable issues of these documents shall be those in effect by the responsible industry association or society on the date of procurement.

- IPC-6011, Generic Performance Specification for Printed Boards
- IPC-6012, Qualification and Performance Specification for Rigid Printed Boards
- IPC-6012FS, Space and Military Avionics Applications Addendum

- IPC-6013, Qualification and Performance Specification for Flexible Printed Boards
- IPC-6018, Qualification and Performance Specification for High Frequency (Microwave) Printed Boards
- IPC-4101, Specification for Base Materials for Rigid and Multilayer Printed Boards
- IPC-4103, Specification for Base Materials for High Speed/High Frequency Applications
- IPC-4203, Cover and Bonding Material for Flexible Printed Circuitry
- IPC-4204, Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Boards
- IPC-4562, Metal Foil for Printed Wiring Applications
- IPC-2221, Generic Standard on Printed Board Design
- IPC-2241, Design Guide for High Speed Controlled Impedance Circuit Boards
- IPC-2222, Sectional Design Standard for Rigid Organic Printed Boards
- IPC-2226, Sectional Design Standard for HDI Printed Boards
- IPC-2251, Design Guide for the Packaging of High Speed Electronic Circuits
- IPC-9252, Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards
- IPC-A-600, Acceptability of Printed Boards
- IPC-D-356, Bare Substrate Electrical Test Data Format
- IPC-SM-840, Qualification and Performance of Permanent Solder Mask
- IPC-TM-650, Test Methods Manual
- ANSI/J-STD-003, Solderability Tests for Printed Boards
- ANSI/J-STD-006, Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications
- ASTM-E595, Standard Test Method for Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in a Vacuum Environment

2.3 ORDER OF PRECEDENCE

The following order of precedence shall apply in the event of a conflict between the procurement document(s), the text of this document and the references cited herein.

1. Contract or purchase order
2. PCB fabrication drawing
3. SEAKR Specification 10079 (*this document*)
4. SEAKR Statement of Work (SOW)
5. IPC Performance Specification (e.g., IPC-6012 or IPC-6013)
6. Other applicable documents (e.g., IPC-A-600, etc.) referenced herein

3 REQUIREMENTS

3.1 GENERAL

PCBs delivered shall be of the material, design, and construction specified on the PO, the drawing and this specification.

In this specification the following terms are used:

- SEAKR Engineering is referred to as SEAKR
- The PCB manufacturer or fabricator is referred to as Fabricator
- The Purchase Order is referred to as PO
- The PCB fabrication drawing is referred to as drawing
- Printed Circuit Board/s are referred to as PCB(s)
- The term “lot” used in text refers to a Production Lot, as defined in **Section 4.5.1.**
- When several IPC performance specification are listed (e.g., IPC-6012 or IPC-6013) for a requirement, use IPC-6012 for PCBs that have no IPC-4204 flex material in the design.

3.1.1 Data Exchange and Verification

3.1.1.1 General Outline

Following is an outline and flow chart of the procedures for Request for Quote (RFQ), Order placement, Data Exchange, Review and Approval.

1. SEAKR Supply Chain sends PDF files to Fabricator for quotation
2. Fabricator completes the quotation
3. SEAKR Supply Chain places PO
4. SEAKR Layout sends master pattern data and drawing to Fabricator
5. Fabricator imports master pattern data (Gerber or ODB++ format) into their system and outputs data (uncompensated, Gerber format). Data sent to **layout@seakr.com** for review
6. Fabricator to create Gerber extracted net list if applicable, and send to **layout@seakr.com** for review (Note: This is not required if Fabricator uses SEAKR supplied net list or ODB++ data)
7. Fabricator to perform a DFM and report results and recommendations on the provided design files and drawing. DFM report shall be sent to **layout@seakr.com** for review
8. Fabricator to create a proposed stackup including adjustments for impedance. Stackup sent to **layout@seakr.com** for review
9. SEAKR verifies data and stackup and replies to DFM issues
10. If the PCB has microvias, the Fabricator shall also send panel data for review
11. When all issues are resolved, SEAKR gives final approval to build

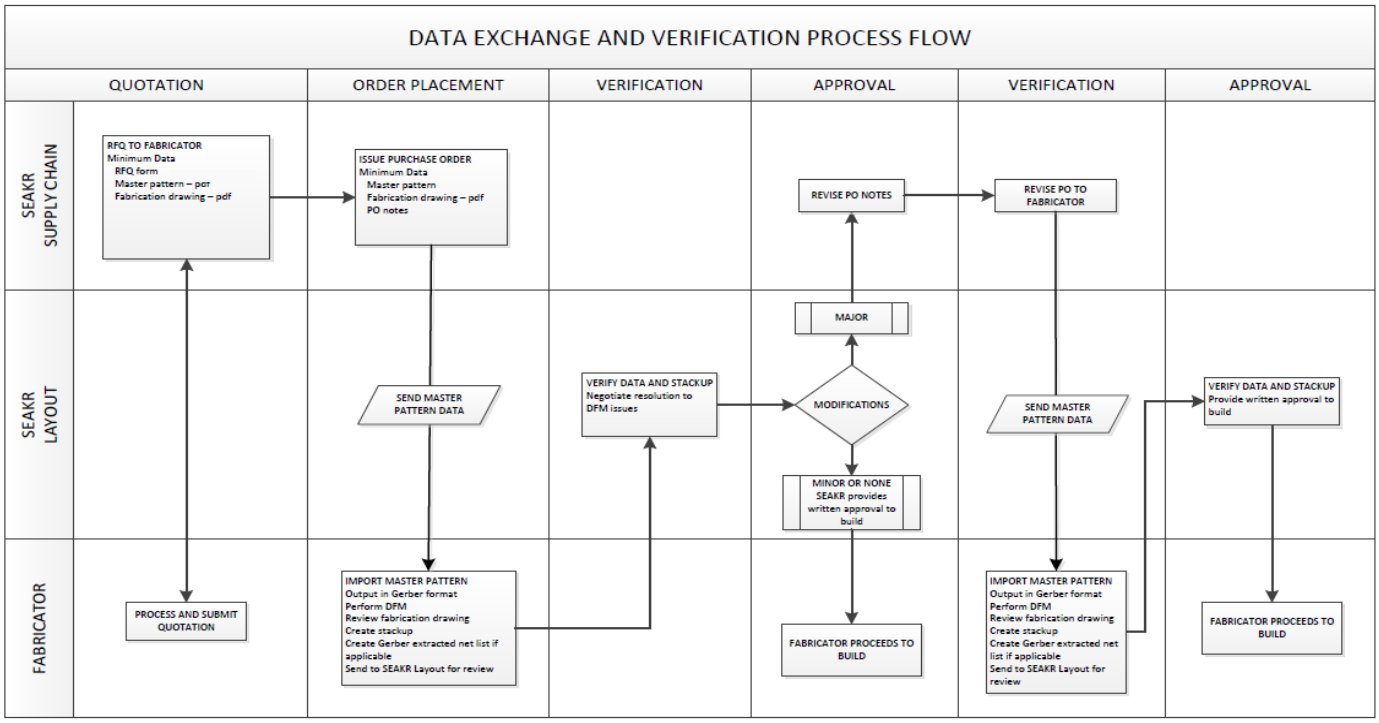

Figure 3-1: Data Exchange and Verification Swim Lane

3.1.1.2 Request for Quote

Prospective Fabricators will be supplied with a RFQ file. This file is for quoting purposes only and shall not be used in fabrication of the actual PCB. Gerber or ODB++ data may be supplied if requested by the Fabricator for quoting purposes only. At a minimum, the RFQ files shall contain the following information:

1. Master pattern (Adobe Acrobat format)
2. Drawing (Adobe Acrobat format)

3.1.1.3 Master Pattern Data

Once a Fabricator is selected, a master pattern data file and a drawing data file will be sent by SEAKR Layout. As a minimum, the files shall contain the following information:

1. Master pattern (in one of the following formats)
    A. ODB++ format – Compressed "tgz" file containing ODB++ database
    B. Gerber format – Compressed "zip" file containing Gerber data, NC drill data, and IPC-D-356 test netlist data
2. Drawing (Adobe Acrobat format)

3.1.1.4 Master Pattern Data Verification

The Fabricator shall import the master pattern data into their system and shall output the artwork to be sent electronically to SEAKR by email (**layout@seakr.com**) for verification.

The artwork shall include all conductive layers, silkscreen(s), and solder masks in Gerber format. The artwork shall represent finished PCB and shall not be compensated for fabrication processes.

If required by PO, the fabricator shall provide panelized working artwork in Gerber format, including all required coupons, before SEAKR will provide final approval, per **Section 3.1.1.10**.

3.1.1.5 Design for Manufacturing (DFM) Report

The Fabricator shall perform DFM on the design prior to starting to set-up or tool the order and report all findings that may adversely affect fabrication, design integrity, or yield. The report shall document the nature and locations of the findings and include a recommendation to correct the findings or eliminate the impact of the findings. The Fabricator shall not proceed to correct any of the noted findings without written approval from SEAKR.

3.1.1.6 Stackup

The stackup detail listed on the drawing shall be used by the Fabricator to generate a fabrication stackup and shall include the following:

1. Finished copper weights
2. Dielectric thicknesses
3. Prepreg style and number of plies, if specified on the drawing
4. Core style and number of plies, if specified on the drawing
5. Impedance control requirements
6. Impedance control trace widths, spaces, and planes referenced
7. Solder mask thicknesses
8. Overall PCB thickness

3.1.1.7 Adjustments for Impedance Control

In order to achieve required impedances, adjustments may be made to trace widths and spacing, and dielectric thicknesses. Trace widths, spacing and dielectric thicknesses may only be adjusted +/- 0.001 inch from the supplied data. Unless specified on the drawing, no trace width shall be below 0.003 inch and no dielectric thickness shall be below 0.0035 inch. Impedance tolerance shall be +/-10% for internal layers and +/-15% for external layers, as listed by layer on the drawing. Core locations shall not be changed. The adjusted trace width, space and dielectric thickness shall be on the manufacturer's stackup. Finished printed board thickness shall be measured over copper plating and solder mask. Thickness tolerance shall be +/-10% of nominal dimension as specified on the stackup detail of the drawing.

3.1.1.8 Net list – IPC D-356 vs. Gerber Extract

If the Fabricator is unable to use the supplied net list in its unaltered form, a net list may be extracted from the Gerber data and used.

The extracted Gerber net list shall be in accordance with IPC-9252 5.1.2 CAD Data Test and shall be verified by SEAKR and written approval is required before proceeding.

3.1.1.9 Corrections and Modifications

If the Fabricator identifies any findings, or improvements required, to make the PCB more manufacturable, it may be necessary to modify the master pattern data, stackup, and/or drawing. The Fabricator shall not make any modifications outside of those described in this specification without written approval from SEAKR. All major modifications and some minor modifications shall be done at SEAKR, resulting in revised data. The Fabricator imports the revised data into their system and exports new data that shall be sent to SEAKR for review, verification, and written approval. The degree of modification (minor or major) dictates whether a completely new data

package or only the affected files will be sent. Some minor modifications may be done at the Fabricator with written approval from SEAKR. Minor modifications performed by the Fabricator and approved by SEAKR shall be noted on the PO.

3.1.1.9.1 Minor Modifications

In the event minor modifications are required, either the changes will be made at SEAKR and only the affected files resent to the Fabricator or SEAKR will authorize the Fabricator, via the PO, to make the changes. The Fabricator is required to resubmit any new artwork data back to SEAKR for review and approval.

Minor modifications to the master pattern are ones that do not affect multiple layers of the circuitry, such as rerouting a trace or correcting solder mask or silkscreen layers. Changes to the drawing or test net list also are considered minor modifications.

3.1.1.9.2 Major Modifications

In the event major modifications are required, the changes will be made at SEAKR and all files will be resent to the Fabricator. The Fabricator is then required to resubmit data to SEAKR for full review, verification and written approval.

Major modifications to the master pattern are ones that affect multiple layers of the circuitry such as adding components or moving vias.

3.1.1.9.3 Isolated Copper (Thieving or Balancing Copper)

All conductors and conductor patterns in SEAKR supplied data are tied to a voltage potential or a mounting hole that connects to chassis ground. Unconnected (floating) copper is verified by SEAKR via the Design Rule Check (DRC) and prior to engagement with the Fabricator. Floating metal is not allowed in some space applications. In the event floating copper is identified in design by the Fabricator by any means, Fabricator shall immediately notify SEAKR and proceed as directed.

In cases where the copper distribution on a layer is not uniform, the Fabricator may add thieving or balancing copper which is not connected to any net with the following conditions:

1. The surface area of each individual copper area shall not exceed 0.3 square centimeters
2. Check plot (Gerber data) of the modified layers shall be sent to SEAKR for review, verification, and written approval

3.1.1.10 Final Approval

After the Fabricator's data (including Gerber extracted net list, if used), DFM report, and stackup have been reviewed and all potential problems resolved, SEAKR will provide the Fabricator with final approval, in writing, to proceed to build the PCB.

Proceeding with fabrication prior to final approval is not permitted.

3.1.1.11 Tolerance of PCB Design

Master pattern (artwork) data supplied is finished (non-compensated) data and represents the finished PCB. The only adjustments to this data allowed, outside of the tolerances cited herein, are to compensate for processes required to fabricate the PCB. These adjustments shall not affect the finished PCB pattern dimensional characteristics.

3.1.1.12 Netlist Verification (Recommended)

Prior to start of fabrication a net compare should be performed to verify that the SEAKR provided net list matches a net list extracted from the final edited data used to create the PCB tooling artwork.

3.1.2 Coupons

3.1.2.1 PCB Manufacturer's Test Coupon Design Requirements

For all classes of product, the A and Bs test coupons shall conform to the requirements of IPC-2221, Appendix B and reflect the specific board characteristics, which are plated through hole construction (e.g., blind and buried vias, microvias, and unfilled or filled holes), backdrills, and the plating steps, in accordance with IPC-6012 or IPC-6013. The A/B coupon design shall only be used for the plated holes that go through the entire thickness of the board. A minimum of two coupons of each type shall be located on opposite corners of the panel. Test coupons shall be designed such that traceability to the panel and each PCB and location shall be easily identified.

On all IPC-6012 or IPC-6013, Class 3 and all IPC-6012FS designs, the fabricator shall supply an **additional** set of coupons of sufficient quantity for as-received and thermal stress testing. These are for third party testing of PCB structural integrity. The coupon set shall contain A, all Bs, S, M, and G coupons on the same strip.

Identify all coupons per **Section 3.5.3.**

3.1.2.2 Impedance Test Coupons

Impedance test coupons shall conform to IPC-2221, IPC-2241, and IPC-2251. Identify coupons per **Section 3.5.3**

3.1.2.3 IST Coupon Testing

If Interconnect Stress Test (IST) coupons are required, it shall be noted on the PO and IST coupon designs will be provided in a separate data package. IST coupon testing requirements shall be included with the IST coupon data package. SEAKR-SOW-230 specifies testing parameters, report format and failure analysis. The PO will provide any additional testing or shipping requirements. Identify coupons per **Section 3.5.3.**

3.1.2.4 IPC D Coupon Testing

For all designs that contain microvias, D coupon testing is required. The PO will provide the applicable Statement of Work that specifies the required test coupons, testing parameters, failure analysis, and report format. SEAKR D coupons will be provided in a separate data package by SEAKR. Identify SEAKR D Coupons per **Section 3.5.3**

Table 3-1: D Coupon and Thermal Shock Test Requirements

Laminate	Statement of Work Document
Megtron 4	SEAKR-SOW-207
Megtron 4S	SEAKR-SOW-208
Megtron 6/6N	SEAKR-SOW-209
Polyimide	SEAKR-SOW-210
Tachyon 100G	SEAKR-SOW-211
Tachyon 100G/Astra MT77	SEAKR-SOW-212

3.1.2.5 SIQC Coupons

If Signal Integrity Qualification Coupons (SIQC) coupons are required, it shall be noted on the PO and SIQC designs will be provided in a separate data package. The fabricator shall deliver the SIQC coupons to SEAKR for analysis. Identify coupons per Section 3.5.3.

3.1.3 Outgassing

Certified test data provided by the material manufacturer and/or by an approved test laboratory shall be reviewed and maintained on all organic materials to verify the following: No material shall have a total mass loss (TML) greater than 1.0% and a collected volatile condensable material (CVCM) greater than 0.10%. All material used in the fabrication (for example, laminate material and solder mask) shall be tested separately. Foil shall be removed from laminate material prior to test. Testing shall be in accordance with ASTM E595.

3.1.4 Laminates

The required laminate material shall be in accordance with the drawing. Rigid metal clad laminates, rigid unclad laminates and bonding material (prepreg) shall be selected from IPC-4101 or IPC-4103. Flexible metal clad laminates, flexible unclad laminates, and bonding material (prepreg) shall be selected from IPC-4204. Laminates used in designs requiring multiple lamination cycles (blind/buried vias) should be selected from the same vendor date code for improved control of material movement.

3.1.4.1 Polyimide

The polyimide laminate used on all PCBs shall meet the requirements of IPC-4101/41. The drawing may indicate a specific material.

3.1.4.2 Tachyon-100G and ASTRA MT77

The Isola Tachyon-100G and/or Astra MT77 laminate used on all PCBs shall meet the requirements of IPC-4103/17. The drawing may indicate a specific material.

3.1.4.3 Megtron 6/6N

The Panasonic Megtron 6/6N laminate used on all PCBs shall meet the requirements of IPC-4101/102 or IPC-4101/91. The drawing may indicate a specific material.

3.1.4.4 FR-4

The FR-4 laminate used on all PCBs shall meet the requirements of IPC-4101/21 or IPC-4101/24. The drawing may indicate a specific material.

3.1.4.5 Flexible (Flex) Laminate

The flex material used on all PCBS shall meet the requirements of IPC-4204/11. The drawing may indicate a specific material.

3.1.4.6 No Flow Prepreg

The no flow prepreg material used on all PCBS shall meet the requirements of IPC-4101/40, IPC-4101/41, or IPC-4101/42. The drawing may indicate a specific material.

3.1.5 Copper Foil

The copper foil used on all PCBs shall be IPC-4562/3, high temperature elongation (HTE). Copper foil thickness (or weights) are listed on the drawing. Internal layers not plated are starting copper. Internal and External layers that are plated are starting copper plus plating. Finished thickness shall be in accordance with IPC-6012 or IPC-6013.

3.1.5.1 Coverlay Material

The coverlay material used on the flexible portion of PCBS shall meet the requirements of IPC-4203/1. The drawing may indicate a specific material.

3.1.6 Metallic Coatings

3.1.6.1 Electrodeposited (Electrolytic) Copper

Electrodeposited copper plating properties, including purity, tensile strength and elongation for all Class 3 and IPC-6012FS PCBs shall be in accordance with IPC-6012FS. Electrodeposited copper plating properties for Class 2 PCBs shall be in accordance with IPC-6012 or IPC-6013. Testing frequency shall comply with the appropriate class in accordance with IPC-6012 or IPC-6013 (**Section 4.4**)

3.1.6.2 Solder Coating

Solder coating shall be by hot air solder leveling (HASL) and the solder procured shall be in accordance with composition Sn63Pb37 of ANSI/J-STD-006. Solder coating coverage shall meet IPC-6012 or IPC-6013 requirements, **Section 3.1.6.1,** and surface mount solderability per ANSI/J-STD-003 edge dip test method using IPC-2221 Appendix B Legacy M or W coupons. The immersion depth 'mark' is not required. Immerse the M or W coupon in the solder to fulfill the contact wetting angle acceptance criteria on the largest solderable feature. Accelerated conditioning and durability tests are not required.

When the ANSI/J-STD-003 solder float test method is done using the M or W coupon, both sides of the test specimen shall be floated on the solder and evaluated for surface mount solderability.

3.1.6.3 Electroless Nickel / Electroless Palladium / Immersion Gold (ENEPIG)

Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) plating deposit and deposit thickness shall be in accordance with IPC-4556. Measurement methodology shall be by XRF spectrometry. Frequency of sample thickness measurements per lot shall be in accordance with Table 4-3 of IPC-6012 or IPC-6013. Thickness measurements shall be made on both sides of the panel.

3.1.7 Organic Coatings

3.1.7.1 Solder Mask

Both outer layers of the PCB shall have green solder mask over bare copper (SMOBC) per IPC-SM-840 Class H, unless specified by drawing. Cleanliness requirements of **Section 3.8** shall be met prior to solder masking. Cleanliness results prior to solder mask are required. The type of solder mask, LPI and/or dry film, shall be specified on the drawing.

3.1.7.1.1 Liquid Photoimageable (LPI)

Only the following LPI solder masks are approved for use (no exceptions allowed without written SEAKR approval, or unless an alternative material is indicated directly by the engineering drawing):

1. Dynachem Epic 200
2. Enthone DSR or SR1000
3. Hysol SR1000

4. Peters SD 2467
5. Taiyo PSR 4000 MP
6. Taiyo PSR 4000 BN
7. Taiyo PSR 4000 LDI
8. Taiyo PSR 4000 HFX

3.1.7.1.2 Dry Film

Dry film solder mask will be sent to SEAKR for written approval prior to use or incorporation in builds.

3.1.8 Via Fill

Unless otherwise specified, only non-conductive via fill material shall be used. Via fill paste (uncured) shall be stored in accordance with the manufacturer's specification.

3.1.8.1 Non-conductive Via Fill

Only the following non-conductive via fill materials are approved for use (no exceptions allowed without written SEAKR approval):

1. San-ei Kagaku PHP-900 IR-10F
2. Taiyo THP-100DX-1
3. San-ei Kagaku PHP-900 IR-6P

3.1.8.2 Conductive Via Fill

Only the following conductive via fill materials are approved for use (no exceptions allowed without written SEAKR approval):

1. Dupont CB100
2. Tatsuta AE3030

3.1.8.3 Copper Via Fill (Microvias)

Microvias shall be copper filled, There are no exceptions allowed without written SEAKR approval.

3.1.9 Marking Ink

Marking ink shall meet the requirements of IPC-4781, be white, nonconductive, permanent, non-nutrient, polymer ink. The use of labels shall not be permitted on boards or coupons.

3.1.10 Material Handling and Storage

Material handling and storage shall be in accordance with applicable manufacturer's data sheets. Raw material storage and handling shall be controlled to ensure and prolong shelf life. For shelf life sensitive materials, a First-in, First-out (FIFO) stock rotation plans shall be used and shelf life expiration dates will be marked on the container (e.g., bags and/or buckets). Expired or re-certified materials shall not be used for SEAKR product. When released from primary storage areas, material shall be handled and controlled to minimize contamination and damage per IPC-1602.

3.1.11 Prohibited Materials

Delivered product shall not contain the following prohibited materials: pure unalloyed tin, tin alloy containing more than 97% tin, cadmium, zinc or unplated brass.

3.2 VISUAL EXAMINATION

The boards shall be visually examined to verify that the design, construction, physical dimensions, markings and workmanship are in accordance with the requirements of the PO, the drawing, this specification, IPC-6012 or IPC-6013, and, when required, IPC-6012FS. IPC-A-600 shall be used as a guideline for acceptability. In the event of conflict between these documents, reference the order of precedence as defined in **Section 2.3**.

For all Class 3 and IPC-6012FS PCBs, 100% of the boards shall be visually inspected; Class 2 visual inspection shall be per IPC-6012 or IPC-6013. The AS9102 compliance report shall be done on at least one (1) board serial number on all new builds shipped to SEAKR. Repeat builds do not require an AS9102 compliance report unless otherwise stated on procurement documentation. Repeat builds require a dimensional report provided to SEAKR, either a CMM report or equivalent. PCBs shall be visually inspected at a magnification from 7X to 10X. Visual inspection of microvia structures shall be conducted at 30X minimum. Magnification up to 40X may be used to referee findings.

3.2.1 External Surfaces

1. Pink ring is not permitted
2. Measling is not permitted
3. Crazing is not permitted
4. Delamination, external laminate cracks, and blistering are not permitted for Class 3 and IPC-6012FS boards. Delamination, external laminate cracks, and blistering shall be per IPC-6012 or IPC-6013 for Class 2 product.
5. Exposed weave and disrupted fibers are not permitted on Class 3 and IPC-6012FS product. Weave exposure shall be per IPC-6012 or IPC-6013 for Class 2 product.
6. There shall be no voids in the copper or solder coating of surface mount lands
7. Soldering coating and coverage requirements (dewetting, nonwetting, and pooling) shall comply with the criteria of **Section 3.1.6.2**.
8. No evidence of metal slivers or solder mask on tape when board is tested per IPC-TM-650-Method 2.4.1.
9. Any combination of isolated surface anomalies (e.g., nicks, dents, nodules or pinholes) within the pristine area are acceptable provided final finish requirements are met, that they are within the dimple/protrusion limits of IPC-6012 3.5.4.8 and 3.5.4.9, and that they do not occupy more than 5% of the pad area.

3.2.2 Edges, Cutouts and Notches

Edges, cutouts, and notches shall be clean cut and without burrs. Nicks and haloing in non-plated through holes, edges, cutouts and notches are acceptable provided the penetration does not violate the required minimum lateral spacing of the PCB. Radius for internal corners shall be 0.031 inch maximum.

3.2.3 Marking Locations

No marking produced through silkscreen, rubber stamp, or stencil shall touch or be placed on exposed conductors, ground planes, or other exposed metallic surfaces. Etched markings are acceptable on the board providing electrical integrity is not compromised. At least 0.005 inch clearance (including nonconductive marking material) shall be maintained between the marking and any part of the etched circuit exposed by the solder mask.

3.2.4 Required Markings

The required markings are supplied on the silkscreen layer(s) from the master pattern data. Additional marking, such as those required for identification purposes shall be applied as specified on the drawing.

3.2.5 Marking Height

Minimum character height is 0.035 inch with a line width of 0.005 inch. In cases where text on the supplied silkscreen layers falls below 0.035 inch or has a line width of less than 0.005 inch, the Fabricator may remove the text from the silkscreen layer.

3.2.6 Workmanship

PCBs shall be processed in a manner as to be uniform in quality and show no evidence of foreign materials. Lifting or separation of plating from the surface of the conductive pattern or from the conductor to the base laminate is not permitted. There shall be no evidence of scratches or damage to the board in excess of those allowed by IPC-A-600.

3.3 DIMENSIONAL REQUIREMENTS

Dimensional requirements and sample plans shall be in accordance with IPC-6012 or IPC-6013, and when required, IPC-6012FS.

3.3.1 Bow and Twist

Maximum bow and twist shall not exceed 0.75% for Class 3 and IPC-6012FS boards. The bow and twist requirement for all Class 2 boards shall be in accordance with IPC-6012.

3.3.2 Board Size

Overall board size tolerance shall be +/-0.020 inch unless otherwise stated on the drawing.

3.3.3 Hole Sizes

Hole sizes are found in the master pattern data and on the drawing. All component through holes are finished hole diameters after drilling and plating. All vias (through, blind, buried, microvias) are drill diameters. Finished hole size for vias is not controlled.

Only new drill bits shall be used. Re-sharpened drill bits are not allowed. The maximum number of hits shall not exceed 500 per drill bit.

3.3.4 Component Holes (Compliant Pin)

These holes are designed to accept compliant pin (press fit) component leads. Tolerance is +/-0.002 inch and shall be measured after copper plating and prior to solder coating.

3.3.5 Minimum Copper Plating Thicknesses

Plating thickness for all plated through holes, through vias, blind and buried vias, and surface copper shall be in accordance with **Table 3-1**.

Copper Thickness in Through Holes, Through Vias, Blind and Buried Vias and Copper Wrap (inch)			
Criteria	**Class 2**	**Class 3**	**IPC-6012FS**
Minimum Average	0.000787	0.00098 Absolute minimum	0.00098 Absolute minimum
Isolated Thin Areas	0.000709	0.00098 Absolute minimum	0.00098 Absolute minimum
Wrap	0.000197	0.000197	0.000197

Table 3-1 : Copper Thickness Requirements

3.3.6 Copper Filled Microvias

Copper filled microvias shall meet the requirements of IPC-6012 or IPC-6013.

3.3.7 Vias (Blind, Buried or Through)

All vias shall be filled in accordance with approved material. Blind and through vias shall be copper capped and meet the appropriate wrap requirements. Voids in cap plating are not permitted.

3.3.8 External Annular Ring

External annular ring shall be per IPC-6012FS for Class 3 and IPC-6012FS product. External annular ring for Class 2 product shall comply with the requirements of IPC-6012 or IPC-6013 for that class. External annular ring assessment of blind and buried vias shall be determined by microsection evaluation.

Sampling for annular ring on a per lot basis shall be in accordance with **Section 3.3**

3.3.9 Etchback

Evidence of etchback shall be required on all plated through-holes and vias for IPC-6012F Class 3 and IPC-6012FS boards. Etchback shall have a minimum depth of .00005” with no more than two layers per hole showing zero etchback. Shadowing is permitted on one side of each land. Maximum etchback shall comply with IPC-6012, IPC-6012 and/or IPC-6012FS.

At a minimum, smear removal is required on Class 2 boards, as etchback is not required.

3.3.10 Wicking

Wicking allowance for all product shall comply with the applicable requirements of IPC-6012, IPC-6013, and/or IPC-6012FS for each class.

3.3.11 Copper Penetration (Dielectric Removal)

The combination of dielectric removal from etchback plus wicking allowance shall not exceed the sum of the maximum allowable etchback or smear removal and the maximum allowable wicking limits defined by IPC-6012, IPC-6013, and/or IPC-6012FS for each applicable class.

3.3.12 Back-Drilled Component Holes and Vias

Fabricator shall select drill size and adjust entry side pads so that pads are removed. Stub length from the no-cut (target) layer shall be 0.008" +/-0.006". Component holes shall be back-drilled after application of board surface finish. Back-drilled component holes and vias shall be inspected to be clear of debris and burrs. Back-drilled vias shall be filled in accordance with approved material. Non-metallic burrs on surrounding laminate are acceptable provided they are firmly attached and immovable.

Solder balls in back-drilled component holes shall be allowed with the following conditions. The solder ball shall not reduce the diameter of the plated hole >75%. For solder balls that reduce the plated hole diameter <= 75%, the solder ball shall be attached to the copper plate. Insert a pin gage into the portion of the hole that is plated and push on the solder ball. The solder ball shall not be removed by the pin gage.

3.4 CONDUCTOR DEFINITION

3.4.1 Conductor Width and Spacing

Boards shall be visually inspected at a magnification from 7X to 10X to verify conductor spacing. Magnification up to 40X may be used to referee findings. Conductor width and spacing shall be within +/-20% of the master pattern.

Impedance control traces may require tighter tolerances and are governed by the Fabricator's process and impedance test results. Inner layers with traces or functional pads shall be 100% inspected at AOI.

3.4.2 Conductor Thickness

Minimum internal layer foil thickness and external conductor thickness after plating (including external layers of buried via cores) shall be in accordance with IPC-6012 or IPC-6013.

3.4.3 Nonfunctional Lands (Internal Layers)

Nonfunctional lands shall not be removed by the Fabricator.

3.4.4 Annular Ring

Internal annular ring shall meet the requirements of IPC-6012, IPC-6013, and/or IPC-6012FS for each class. Inspection shall be in accordance with IPC-6012FS for Class 3 and IPC-6012FS boards (per panel).

External annular ring shall meet the requirements of IPC-6012, IPC-6013, and/or IPC-6012FS for each class of product. Inspection shall be in accordance with IPC-6012FS for Class 3 and IPC-6012FS boards (per PCB). External annular ring assessment shall not be done by microsection evaluation.

3.5 STRUCTURAL INTEGRITY

3.5.1 Test Coupon Requirements

3.5.1.1 Fabricator Microsection

The coupons in **Section 3.1.2.1** shall be used for structural integrity compliance tested. The coupons shall not be separated from the panel prior to completing all PCB manufacturing processes. A 100% coupon evaluation in accordance with IPC-6012FS for each panel is required.

3.5.1.2 Third Party Test

Microsection For all Class 3, and IPC-6012FS orders, the Fabricator shall provide a coupon set for each panel sufficient for as-received and post-thermal stress testing and in accordance with the requirements of **Section 3.1.2**. A set shall contain A, all Bs, S, M or W, and G coupons on the same strip. At the same time the Fabricator ships the Class 3 or IPC-6012FS PCBs (including impedance coupons) to SEAKR, the Fabricator shall also ship the corresponding complete set of coupons to the third party test lab specified on the PO.

3.5.1.3 Third Party Test DPA Board

If directed by the PO, the Fabricator shall send the third party test lab a PCB from one of the same panels as the submitted fabrication test coupons. Non-compliant or thermally stressed PCBs shall not be used for this purpose, without prior written approval from SEAKR. If multiple production lots are shipped, as defined in **Section 4.5.1**, a DPA is required for each production lot.

3.5.2 Test Method

If required by PO, NASA-RP-1161 shall be used to provide guidance in preparing and inspecting coupons.

3.5.2.1 Fabricator

The evaluation shall be performed per IPC-6012. Thermal stress twice on each side (4 times total) per IPC-TM-650, Method 2.6.8, Condition A. For printed circuit boards utilizing microvias, the microvias in the test coupon(s) or printed board shall be in contact with the solder when floated. If microvias exist on both sides of the printed board design, representative test coupon(s) or printed board(s) shall be individually floated for each side with microvias prior to cross-section evaluations. If microsections are prepared individually for each side, the thermal stress need only be performed on the side to be evaluated.

3.5.2.2 Third Party Test

The Class 3 or IPC-6012FS third party evaluation shall be performed, as-received, per IPC-TM-650, Test Method 2.1.1 and after two cycles of thermal stress, per IPC-TM-650, Method 2.6.8, Test Condition A. Note that a single thermal stress cycle is herein defined as one float exposure on each side of the coupon, and coupons shall be allowed to cool to room temperature in between each thermal stress float.

A representative photo of each plated drill type, and one photo of each drill structure that violates the requirements of the acceptance criteria of the PCB specification and classification referenced on the PO shall be taken at the following conditions:

- As received before etch (does not apply to microvias)
- As received after etch (does not apply to microvias)
- Thermally stressed before etch
- Thermally stressed after etch
- The representative photo shall show the both sides of the plated hole along the entire length of the hole.
- Polarization light should be used if microvia separation is suspected
- If microvia separation is suspected or other out of specification (OOS) condition for a microvia structure is determined, then the final report for this OOS condition shall include all representative photos for the microvia structure both before and after etch.

- If no microvia separation is suspected and no other OOS conditions are determined for the microvia structure type, then only one photo of a via before etch and after etch is required in the final report.
- If a through-hole, buried and blind via out of specification (OOS) condition is determined, representative photos shall sufficiently capture the OOS condition and be included in the final report. Only one photo of each via structure before etch and after etch is necessary if an OOS condition is not identified.

Failure of the third party test lab analysis shall result in rejection of the corresponding PCBs and/or lot.

Requirements for Microsectioned Coupons (Fabricator and 3rd Party)

Microsections shall be evaluated both before and after etching.

PTH (including buried and blind vias) shall be examined at a magnification of 100X, referee up to 200X.

Microvias shall be examined at a magnification of 200X, referee up to 500X.

Microsections for all classes of product shall comply with the applicable criteria of IPC-6012, IPC-6013 and/or IPC-6012FS, except where alternative criteria is provided below:

- Copper plating thicknesses shall be in accordance with **Section 3.3.5**, **3.3.6**, and **Table 3-1**.
- Etchback shall be per **Section 3.3.9**
- Blind, buried and through vias shall be a minimum of 85% filled and in accordance with **Section 3.3.7**.
- Voids in cap plating are not permitted
- Plating folds and inclusions shall meet the minimum copper thickness requirements defined in **Table 3-1**
- In the as received coupon, laminate voids and/or cracks shall not exceed 0.003 inch. There shall be no lifted lands. Resin recession shall not exceed 0.003 inch deep or 40% of the dielectric thickness along the length of the drilled hole (i.e., PCB thickness minus to copper thickness [foil and/or plating])
- After thermal stress, lifted lands shall not exceed the thickness of the foil. Lifted lands for blind microvias are not permitted after thermal stress.
- Copper wrap requirements for shall be in accordance with **Table 3-1**. Microvias that are copper filled are exempt from copper wrap requirements when over plated with 0.0002 inch minimum copper.
- On the outer layer of buried via cores, type A foil cracks are acceptable for all classes. Type B foil cracks are acceptable for Class 2, but are not acceptable for Class 3.
- Separation of the over plate to underlying plating and copper fill shall not be acceptable. The requirements for minimum surface conductor thickness shall also apply.
- Protrusions and depressions shall be evaluated per IPC-6012, IPC-6013 and/or IPC-6012FS with the exception that hole-fill material between microvia plating and overplate shall be cause for rejection.

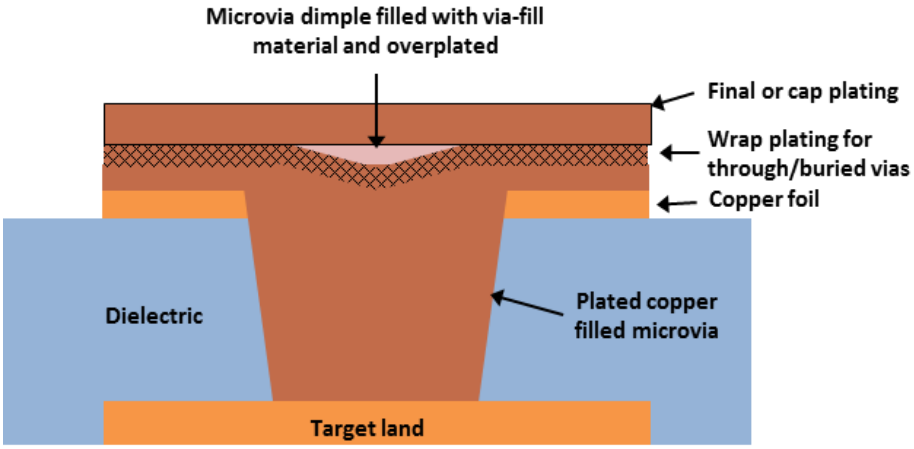

Figure 3-2: Unacceptable Microvia Dimple

- Dielectric removal and wicking shall be per **Section 3.3.10** and **Section 3.3.11**.
- Backdrill holes shall be per **Section 3.3.12**.

3.5.3 Test Coupon Identification

Test coupons, including impedance control coupons, shall be identified with the following:

1. FSCM of Fabricator
2. Part number and revision level of the drawing
3. PCB traceability and serial lot number identification
4. Fabricator Panel Number identification

3.5.4 Coupon Retention

The Fabricator shall retain all coupon cross-sections (except those provided to SEAKR) at their facility for a minimum of 3 years. Fabricator shall supply and maintain documentation that links the cross sections to the manufacturing panel.

3.6 Solder Mask Requirements

3.6.1 Coverage and Clearance

Unless otherwise dictated by design, solder mask shall not encroach on or cover any land. Solder mask may be tangent to the land, except BGA land patterns. BGA land patterns shall have a minimum 0.001 inch clearance between solder mask and land.

3.6.2 LPI

Thickness over conductors shall be 0.0005 inch to 0.002 inch as measured on coupon G by the Fabricator. Solder mask shall exist between all lands and cover all vias. Thickness measurements shall be retained in the manufacturing for each lot of PCBs.

3.6.3 Dry Film

Thickness over conductors shall be 0.004 inch maximum as measured on coupon G by the Fabricator. Solder mask shall tent or cover all vias, providing an airtight seal. Thickness measurement shall be retained in the manufacturing for each lot of PCBs.

3.7 ELECTRICAL REQUIREMENTS

3.7.1 Bare Board Testing

Bare board testing shall be performed in accordance with IPC-9252 and IPC-6012 or IPC-6013. The resistive test method used shall verify each board against the net list (IPC-D-356 or ODB++ file format) supplied by SEAKR with the master pattern data, or the approved Gerber extracted net list (see **Section 3.1.1.12**).Basic electrical testing includes 100% continuity and isolation per **Table 3-2**.

3.7.2 Hi-Pot Testing

If Hi-Pot testing is required per PO or drawing, testing shall be performed in accordance with IPC-TM-650, method 2.5.7, Condition A unless otherwise specified. Hi-pot certification required.

Phase testing or indirect test by signature comparison is NOT permitted.

Electrical Testing Values			
Test	**Class 2**	**Class 3**	**IPC-6012FS**
Continuity	10 VDC*, 50Ω max	10VDC*, 10Ω max	10VDC*, 10Ω max
Isolation	250VDC, 2MΩ min	250VDC, 100MΩ min	250VDC, 100MΩ min
Nets and end points ****	All	All	All

** Current limited to 10 milliamps.*
*** Test points shall be at the end points of each net. Through hole or surface mount land patterns shall be used for test points.*

Table 3-2 : Electrical Testing Values

3.7.3 Controlled Impedance

3.7.3.1 Impedance Control Verification

Impedance testing shall be in accordance with IPC-6012 or IPC-6013 and conducted on 100% of panels. The Fabricator shall provide time domain reflectometry (TDR) test reports to show compliance with impedance requirements. If SEAKR requires test plots, the requirement shall be listed on the PO or drawing, and on the request for quote.

3.7.3.2 Impedance Tolerance Requirements

Unless otherwise specified on the drawing the impedance tolerance shall be +/-10% for internal layers and +/-15% for external layers.

3.8 CLEANLINESS

There shall be no evidence of dirt, foreign material, oil, finger prints, solder smear transferred to the dielectric surface, solder flux residue or other contaminates that affect life, the ability to assemble, and serviceability. There shall be no loose plating slivers on the surface of the board.

All panels shall undergo a cleanliness test prior to the application of solder mask. Cleanliness testing shall be conducted in accordance with IPC-6012 or IPC-6013 using IPC-TM-650, Method 2.3.25. Cleanliness testing of inner layers after oxide treatment, or of finished boards after solder mask or solder coating, is not required. Cleanliness testing report shall be included.

3.9 REPAIR

No internal or external repairs shall be allowed on any PCB. There shall be no exceptions to this requirement.

3.10 REWORK

The touch-up of surface imperfections in the solder mask, solder, or removal of extraneous copper is permitted providing it does not affect the functional integrity of the board. Epoxy is acceptable for LPI solder mask rework. Epoxy type shall be submitted for approval by SEAKR prior to use. Solder mask touch-up using LPI identical to the original solder mask processing step may be completed without notification to or written approval from SEAKR.

In the event of LPI rework at the fabricator and prior to first delivery of a production lot to SEAKR, test coupons shall undergo baking or additional thermal excursions identical to those experienced by deliverable PCBs, and prior to the fabricator performing microsection analysis.

In the event PCBs are returned to the supplier from SEAKR for rework of LPI, this requirement does not apply (i.e., additional thermal excursions are not required for coupons).

3.11 DESTRUCTIVE PHYSICAL ANALYSIS (DPA)

DPA is required for all IPC-6012FS orders unless a waiver to this requirement is provided on the PO and/or drawing. DPA shall be in accordance with IPC-6012FS. DPA is required per each production lot, as defined by **section 4.5.1.**

4 QUALITY ASSURANCE PROVISIONS

PCBs furnished for SEAKR shall conform to the requirements of the PO, the drawing, this specification, and as applicable IPC-2221, IPC-2222, IPC-6011, IPC-6012, IPC-6012FS, IPC-6013, MIL-PRF-31032, and MIL-PRF-55110.

4.1 FABRICATOR QUALIFICATION

4.1.1 General

Qualification testing is AABUS in accordance with IPC-6012 or IPC-6013. Fabricator shall contact SEAKR on a case-by-case basis in the event qualification is required for agreement of terms prior to conducting any work.

Only facilities that are on the QPL for MIL-PRF-55110 or QML for MIL-PRF-31032 and maintain an ongoing certification can be qualified to this specification, unless qualified by an independent SEAKR audit. The Fabricator shall notify SEAKR if QML or QPL status has changed.

4.1.2 Qualification Validation

The Fabricator's quality assurance validation process shall involve a SEAKR review of the Fabricator's Quality Plan, Validation Plan, and Self-Validation results. The Fabricator shall demonstrate to SEAKR that systems have been implemented and maintained to meet the

requirements of this specification. All of the Fabricator's processes, including contract service operations, may be reviewed. SEAKR shall reserve the right to perform on-site validation surveys of the facilities.

4.2 END ITEM DATA PACK (EIDP)

The EIDP delivered with the finished PCBs to SEAKR, shall be in accordance with AS/EN/SJAC 9102. The following requirements are also summarized in a checklist format, provided in **Appendix III**, for ease of reference and verification. EIDP for each fabrication lot shall contain as a minimum:

- Certificate of Conformance (CofC) with specific statement indicating the compliance to the requirement specified on the drawing.
    - The CofC shall include SEAKR part number/revision, PO number, serial numbers and date code of all PCB's being delivered to SEAKR in the following format XXXX-YYYY, where XXXX is the panel and board serial number format per **Section 4.5.3** and YYYY is the date code four digit format per **Section 4.5.2.**
- Certifications for all materials used in the production of SEAKR PCB's (i.e. laminate, prepreg, copper foil, coverlay, solder mask, via fill, marking ink, and HASL finish). The material certification shall show compliance to the material requirement(s) in **Section 3.1**and list the material lot code(s) used to fabricate the PCB.
    - Ionic contamination certification
    - Via fill certifications shall list one of the approved materials in **Section 3.1.8**.
- **Microsection Report.** The report shall include the SEAKR part number/revision, panel numbers and lot date code of all PCBs associated with the report. The following information (at a minimum) and a statement of compliance is required.
    - Thermal Stress parameters (temperature and number of cycles)
    - Solderability test and acceptance
    - Industry specification and revision for the microsection inspection
    - The inspection results for each item in **Section 0**.
    - Dimensional measurements for **Table 3-1** copper plating thickness, etchback, and backdrill stub lengths (as applicable).
    - Board stack-up measurements (dielectric thickness, copper foil thickness, plated layer thickness).
    - A representative photo of each plated hole type (e.g. through hole and via, buried via, blind via, microvia, backdrill, etc.) that shows both sides of the plated hole and the entire length of the hole. The photo label shall state the coupon type (e.g. A, B, A/B), etch condition (e.g. As-Received or Post Etch), panel number, and photo magnification).

      The backdrill photo shall show the entire length of the hole that copper was removed, the 'No Cut Layer', and the start layer shall be labeled.
- CMM report or equivalent that includes the SEAKR part number/revision, lot date code, serial numbers inspected, drawing PCB dimensional requirements (e.g. size, geometric

dimension, hole diameters, etc.), the dimensional tolerance, the measured value, the tool used to make the measurement, and compliance (e.g. accept/reject).

- Visual report that includes the SEAKR part number/revision, lot date code, industry specification and revision, inspection criteria evaluated and compliance (accept or reject), and a specific statement that 100% of the boards submitted were inspected.
- Electrical test report that includes the SEAKR part number/revision, PO number, lot date code and the following information
    - Test site location name and address
    - Quantity of PCBs tested and accepted
    - Continuity and isolation test values (see **Section 3.7**)
    - Electrical test method used (e.g. resistive)
    - Operator Signature and date.
- Hi-pot report that includes SEAKR part number/revision, PO number, date code and the following information
    - Quantity of PCBs tested and accepted
    - Test voltage
    - Operator Signature and date
- Impedance test report and coupons (TDR plots only required when called out on the PO or drawing). The impedance test report shall include the SEAKR part number/revision, lot date code, and a list of panel number(s) tested. For each panel, the report shall provide the impedance test results (test structure name, target impedance, impedance tolerance, and impedance measurement).
- All applicable SEAKR approved waivers, SEAKR approved PCB stack-up, and any deviation request documentation

Inspection reports, certificates of compliance and test data shall be maintained on file for review by SEAKR quality assurance personnel, as well as SEAKR customers when contractually required.

4.3 ACCEPTANCE

4.3.1 Fabricator's Final Inspection

The Fabricator shall conduct final inspections in accordance with the requirements this specification, IPC-6012, IPC-6013 and/or IPC-6012FS (when applicable). In the event of a conflict, reference **Section 2.3.** Magnification criteria for visual inspection of **Section 3.2** shall apply for all classes of product. All Class 3 and IPC-6012FS PCBs shall be subjected to a 100% test coupon inspection and a 100% visual inspection.

SEAKR reserves the right to reject any/all products not meeting the requirements of this specification.

IPC-A-600 shall be used as a guideline for acceptability.

4.3.2 Disposition of Rejected and Noncompliant PCBs

4.3.2.1 Minor Non-compliance

A minor non-compliance is a defect that does not adversely affect the performance, interchangeability, reliability, maintainability, weight or appearance of the item. In the event that a PCB fails to pass inspection and is not dispositioned as scrap, due to the non-compliance being classified as minor, the Fabricator shall remove the PCB and store it separately from the rest of the lot until resolution is reached (not to exceed 5 business days).

The Fabricator shall notify SEAKR Supply Chain of the non-compliance and request a one-time deviation. The request shall be in a detail and consistently document format that precisely describes the non-compliance including all of the following information:

1. Fabricator's rationale for submittal and justification for SEAKR's acceptance
2. PO
3. Part number and revision
4. Production lot number and number of boards/panels in the lot
5. Quantity of boards/panels rejected from the lot
6. Reference to the specific violation; drawing note, specification and paragraph, and numerical value if applicable
7. Photographs of microsections or visual defects
8. Root cause of the noncompliance (could be preliminary at the time resolution is being sought)
9. Corrective action (could be preliminary at the time resolution is being sought)
10. Recovery time to replace the rejected parts if they are not accepted by SEAKR

The above submitted information must be in sufficient detail for SEAKR to make a timely and informed decision on the disposition.

4.3.2.2 Major Non-compliance

A major non-compliance is a defect which cannot be eliminated by rework or reduced to the level of a minor non-compliance by repair; a significant mulitifacted or multi-example breakdown of quality processes. In the event that a PCB fails to pass inspection and is dispositioned as scrap because the non-compliance is major, the Fabricator shall remove the PCB from the rest of the lot and notify SEAKR for confirmation and/or approval before proceeding with physical scrap.

The Fabricator shall immediately notify SEAKR Supply Chain of the scrap including: the quantity, root cause and corrective action (RCCA), and the schedule recovery time; and the delivery schedule for the remaining non-scrapped boards.

If a major non-compliance is approved for shipment to SEAKR, the PCB must include the documentation in **Section 4.2** with the shipment.

4.3.3 Deviations and Waivers

Deviations and waivers to the PO, drawing, or this specification including the above one time request for deviation shall be submitted to SEAKR for approval. Written approval for any deviation or waiver shall be listed on the PO prior to delivering product and shall be included as part of the standard end item data package.

4.3.4 Source Inspection

SEAKR reserves the right to verify that all the requirements of this specification have been met prior to shipment in accordance with the PO. Periodic surveillance and/or inspection of all phases of fabrication including the subcontractor(s), testing and inspection may be also conducted.

4.3.5 Referee Microsection Test

If referee microsection testing is performed, the fabricator shall notify SEAKR Engineering in writing. The written notification shall include justification per **Section 4.3.2,** a panel layout drawing showing which parts are to be referee microsectioned, and the sample location on the part for all affected panels.

4.4 QUALITY CONFORMANCE TESTING

For Class 3 and IPC-6012FS, quality conformance testing shall be performed monthly in accordance with IPC-6012 or IPC-6013, Class 3 for each type of material (e.g., polyimide, Megtron 6, Tachyon, etc.) that passed acceptance testing. The monthly test shall be on the most complex board for each material type. The board complexity definition shall include multiple laminations and microvias as a board complexity. MIL-PRF Group B testing is an acceptable alternative to the required IPC-6012 or IPC-6013 quality conformance test. Quality conformance testing is not required for Class 2 product. Quality conformance testing shall be performed at a 3rd party lab.

Monthly reports shall be provided to SEAKR on request. The Fabricator shall notify SEAKR immediately on failure of any Quality Conformance Tests.

4.5 SERIALIZATION AND TRACEABILITY

4.5.1 Production Lot

A production lot shall consist of all PCBs having the same part number, lot date code, fabricated from the same materials, using the same processes, produced under the same conditions, accompanied by the same routing documentation and submitted for acceptance inspection at the same time.

4.5.2 Lot Date Code

All PCBs shall be marked by a unique code to identify the period during which PCBs in that lot were manufactured. The marking method used and the time of application of the lot date code shall be defined herein. The first two numbers in the code shall be two digits indicating the calendar week of the year, and the third and fourth numbers shall be the last two digits of the number year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right or from top to bottom, the code number shall designate the week and year, in that order (e.g., 2305 equals week 23 of 2005).

Trailing lot modifiers, critical to maintaining the traceability of inspection lots or split lots, shall be consistently reported on CofCs delivered and the physical markings on the PCBs (e.g., 4420-*01*, 4420-*01.01A*, etc.)

4.5.3 Serialization

Each PCB shall be identified with a unique serial number per lot. The serial number shall be traceable to its panel in the format "P-B" where "P" equals the panel number and "B" equals the board from that panel.

4.5.4 Material Traceability

PCB material traceability shall be such that for each lot of PCBs, all PCB materials specified or used shall be traceable to a material production lot or other specified grouping.

4.5.5 Process Traceability

Each PCB, or each group of PCBs that has been fabricated as a lot, shall be identifiable such that the complete manufacturing history shall be traceable. The history should include, as a minimum, the performance date of all identified production process steps, the procedure specification, any in-process rework steps, any non-conformances including the disposition (e.g., rework, scrap, or SEAKR waiver) and the identification of the equipment used and operator performing the process steps.

4.5.6 Coupon Traceability

The Fabricator shall maintain lot traceability for all PCBs. Each test coupon shall be identifiable with those corresponding PCBs produced on the same panel. All separated individual test coupons shall have their traceability maintained back to the panel or qualification test vehicle from which the test coupons were separated.

4.6 PROCESS CONTROL

The Fabricator shall establish and maintain process controls, quality controls and inspections at appropriately located points in the fabricating process (via production travelers and/or a control plan) to assure continuous control of quality of materials, individual layers, and assembled layers. Process controls will also include procedures relating to contract service operations (outsourced functions/steps), such as deliverable product inspection, contractor audit criteria, and/or testing. These controls and inspections shall be adequate to assure compliance with the PCB procurement documentation and quality requirements of PCBs manufactured to this specification and the associated referenced specifications.

The Fabricator is required to disclose any processes or materials required for SEAKR builds that do not have qualified and validated manufacturing procedures or processes in their fabrication operation. An updated product traveler, test data, and/or control plan that establishes the process, material or process change(s) as qualified product shall be provided to SEAKR as notification. Only materials with qualified processes may be used in SEAKR fabrications. Any new materials or processes that are not qualified in manufacturing require SEAKR approval prior to incorporation into any build. SEAKR will require a review of the experimental design, evaluation plan and validation prior to use in fabrication on, or in SEAKR product.

4.6.1 Process Monitoring

A process monitoring system shall be used by the Fabricator to control key processing steps to insure product yield and process reliability. The monitoring system can use various test vehicles, methods and measurement techniques. The critical operations to be monitored shall be determined by the Fabricator based on their experience and knowledge of their processes. The resulting data shall be analyzed by appropriate process control methods to determine control effectiveness. SEAKR Engineering reserves the right to verify monitoring systems at the supplier's facility at any time during normal working hours to ensure proper implementation and compliance to this specification

4.7 CONTRACT SERVICES / OUTSOURCED SERVICES

SEAKR shall be notified of all subcontracted manufacturing processes in advance of PO acceptance. A subcontractor incudes either a contracted service performed by a third party, or a sister site within the Fabricator's company. The Fabricator shall flow down the applicable requirements of this specification to the subcontractor. The Fabricator assumes all responsibility that the subcontracted service has demonstrated the ability to meet the applicable requirements of this specification. SEAKR reserves the right to audit the Fabricator's subcontractors.

5 PACKAGING AND SHIPPING

5.1 INDIVIDUAL WRAPPING

Each PCB shall be wrapped individually in suitable material and secured in groups to prevent abrasion damage or board edge damage during transport. The wrapping material shall be constructed from material that will not contribute to degraded solderability of the PCB for a one year storage period under normal ambient conditions.

5.2 SHIPPING CONTAINER

The PCBs shall be protected adequately during shipment by using suitable packing materials and placing them in a shipping container or box to support the PCBs during transport.

6 SUPPLIER RESPONSIBILITY

6.1 TRAINING

Training and testing practices shall be employed by the Fabricator to establish, evaluate, and maintain the skills of personnel engaged in production, testing, or inspection of PCBs manufactured for SEAKR. IPC-A-600 or IPC-6012 certifications are preferred. The training program shall be documented as to form, content, and frequency. The Fabricator shall define training requirements which assure operator knowledge of internal standards and proficiency to perform assigned tasks. The methods of updating operators to changes in internal standards and to assure continued proficiency shall be addressed. Records showing the basis of operator acceptability shall be on file including instruction and evaluations received. Records are required only for product related training as distinguished from safety, first aid, etc.

APPENDIX I: IPC-6012 CLASS 3 VS. SEAKR 10079 REQUIREMENTS MATRIX

Characteristic	IPC-6012 Class 3 Requirement		SEAKR 10079 Requirement	
Copper deposition/ Electrodeposited Copper	3.2.6.2	36K PSI tensile, 12% elongation	3.1.6.1	40K PSI tensile, 18% elongation
Crazing	3.3.2.2	≤50% of distance between conductors	3.2	Not permitted
Delamination and Blistering	3.3.2.3	<1% of board area, no propagation under stress, <25% of distance between conductors	3.2	Not permitted
Dewetting, Non-wetting, and Solder Coverage	3.5.4.2.1; 3.5.4.5	Dewetting acceptable in rectangular or circular pad pristine area provided final finish requirements met, <5% of the pad area acceptable dimple/protrusion 5% of surfaces to be soldered	3.2	No dewetting or non-wetting on surfaces to be soldered. Solder coverage for critical features in accordance with 3.1.6.2
Etchback	3.6.2.6	0.0002 - 0.003 inch, 0.0005 inch preferred	3.3.9	Class 3 & Space Addendum: Evidence of Etchback with a minimum depth of .00005” No more than two layers showing zero etchback No Negative Etchback allowed
Electrical continuity and isolation resistance	3.8.2; IPC-9252	Net list test, 40V minimum, 10 megohms minimum, Mid-point testing required.	3.7.1	Net list test, 250V, 100 megohms min. No mid-point testing required.
Material, metal foils	3.2.4	IPC 4562, Foil grade per dwg	3.1.5	IPC 4562, Grade 3 (HTE Copper)
Material fill of through, blind, buried, and microvia structures	3.6.2.19	60% minimum fill. For outer layer surfaces or microvia stacked on buried via, meet dimple and bump requirements if capped	0; 3.1.8.3	Blind, buried, and through hole 85% filled. All microvias are copper filled.
Measling	3.3.2.1	Acceptable	3.2.1	Not permitted
Pink Ring	3.3.2.10	Acceptable	3.2.1	Not permitted

Characteristic	IPC-6012 Class 3 Requirement		SEAKR 10079 Requirement	
Plating thickness	3.6.2.11 Table 3-10 to 3-12	0.000984 inchavg., 0.000787 inch min thin area, Initial Release of Design – before Dec. 31., 2017: 0.000472 inch min wrap Initial Release of Design – after Jan. 1, 2018: 0.000197 inch min. wrap	3.3.5	0.000984 absolute minimum. 0.000197 inch min wrap
Repair	3.11	AABUS	3.9	None allowed
Solder mask thickness	3.7.3	AABUS	3.6	LPI, 0.0005-0.002 inch over laminate. Dry Film, 0.004 inch max. over laminate
Plating hole Integrity after stress	Table 3-9	Sampling Plan 2.5 per Table 4-3	3.5	100% of panels
Structural integrity before thermal stress	None	NA	0	No lifted lands, no resin recession >0.003 inch, no laminate voids >0.003 inch (100% of panels)
Structural integrity after thermal stress	3.6, Table 3-8	All of Table 3-8	0	Third Party Lab: Coupons shall be prepared in both as received and after 2X thermal stress cycles (one cycle is one float exposure on each side of the coupon, cooled to room temperature between floats)
				Class 3 & Space Addendum: Evidence of Etchback with a minimum depth of .00005” No more than two layers showing zero etchback No Negative Etchback allowed
	3.6.2.19; Figure 3-48 & Figure 3-49	When cap plating is not specified for Class 2 and Class 3, fill material within blind and through vias shall seal internal voids from external surfaces and be planar with the surface within ±0.003 inch		Blind, buried and through vias shall be a minimum of 85% filled

Characteristic	IPC-6012 Class 3 Requirement		SEAKR 10079 Requirement	
	3.6.2.10	No lifted lands in blind microvias after thermal stress		Lifted lands shall not exceed the thickness of the copper foil. No lifted lands in blind microvias after thermal stress
	3.6.2.11.1	Wrap requirements for IPC-6012 Class 3 shall be 0.0002 inch minimum for all new designs released after Jan 1., 2018		Wrap requirements for IPC-6012 Class 3 shall be 0.000197 inch minimum in accordance with IPC-6018 Class 3 for all designs
	3.6, Table 3-8	All of Table 3-8		On the outer layer of buried via cores, type A foil cracks are acceptable for all classes. Type B foil cracks are acceptable for class 2, but not for class 3.
				Separation of the overplate to underlying plating and copper fill shall not be acceptable. The requirements for minimum surface conductor thickness shall also apply
				Protrusions and depressions shall be evaluated per IPC-6012, IPC-6013 and/or IPC-6012FS with the exception that hole-fill material between microvia plating and overplate shall be cause for rejection.
Thermal Stress Testing, Method 2.6.8 (Microvias)	3.6.1.1.1	Thermal Stress Testing, Method 2.6.8 (Microvias) - For printed boards utilizing microvias, the microvias shall be in contact with the solder when floated. If microvias exist on both sides of the test coupon or printed board in the test coupon to be evaluated, both sides shall be individually floated and evaluated after thermal stress, either on the same coupon or on individual coupons.	3.1.2.4	Thermal stress coupons 2X on each side of the coupon, 4 times total. Tool and test IPC-2221 D coupons

Characteristic	IPC-6012 Class 3 Requirement		SEAKR 10079 Requirement	
Visual	3.3	Sampling plan for conformance to par 3.3.1 to 3.3.10	3.2	All Class 3 requirements with 100% Inspection
Voids, Laminate	3.6.2.3	For samples exposed to thermal stress, laminate voids between conductive patterns that are not electrically common shall not reduce the minimum dielectric thickness	0	For samples not exposed to thermal stress, laminate voids shall not exceed 0.003 inch.

APPENDIX II: IPC-6012ES VS. SEAKR 10079 REQUIREMENTS MATRIX

Characteristic	IPC-6012FS Requirement		SEAKR 10079 Requirement	
Dewetting, Non-wetting, and Solder Coverage	3.5.4.5	No dewetting on surfaces to be soldered, including surface mount lands. No nonwetting permitted.	3.1.6.2	No dewetting or non-wetting on surfaces to be soldered. Solder coverage for critical features in accordance with 3.1.6.2.
Plating Thickness	Table 3-4 to Table 3-6	Wrap requirements for IPC-6012 Class 3 shall be 0.0002 inch minimum for all new designs released after Jan 1., 2018	3.3.5	Wrap requirements shall be 0.000197 inch minimum
Lifted lands after thermal stress or rework	3.6.2.1 & Table 3-10	Allowed, not to exceed thickness of foil plus plating. No lifted lands on blind microvias	3.5.2	Allowed on thermally stressed microsections, not to exceed thickness of foil plus plating.; **Not permitted on PCBs**. No lifted lands on blind microvias on thermally stressed microsections or PCBs.
Structural Integrity	3.6	When printed boards contain microvias, conformance testing shall include IPC-TM-650 Method 2.6.27. A minimum of one IPC-2221, Appendix A "D" Coupon for each microvia structure shall be tested from each fabrication panel. When a structure includes both microvias and buried vias, the "D" coupons shall include the entire structure. Results are based on resistance change and the microsection requirement of IPC-TM-650 2.6.27 does not apply. Other performance based test methods may be utilized in lieu of IPC-TM-650 Method 2.6.27 for conformance testing of microvia structures, when specified.	3.1.2.4	When the boards contain microvias, the fabricator shall tool the D coupon, subject the coupons to 6 reflow simulations per IPC-TM-650 Method 2.6.27A using the 230C profile. After reflow simulation, the IPC D coupons shall be subject to 100 thermal shock cycles per IPC-TM-650 Method 2.6.7.2. The maximum temperature shall not exceed Tg-10C (190C max) and the low temperature shall be -55C. Thermal shock acceptance criteria shall be <5% change in resistance. Microsection is required per Method 2.6.7.2.

Characteristic	IPC-6012FS Requirement		SEAKR 10079 Requirement	
Thermal Stress Testing Method for Microvias	3.6.1	Thermal Stress Testing, Method 2.6.8 (Microvias) - For printed boards utilizing microvias, the microvias shall be in contact with the solder when floated. If microvias exist on both sides of the test coupon or printed board in the test coupon to be evaluated, both sides shall be individually floated and evaluated after thermal stress, either on the same coupon or on individual coupons.	3.5.1	Thermal stress coupons 2X on each side, 4 times total. Tool and test IPC-2221 D coupons

APPENDIX III: SUPPLIER EIDP VERIFICATION CHECKLIST

Reference **Section 4.2** for complete detail of EIDP requirements. The checklist below is provided for ease of verification and summary of Fabricator submittals.

EIDP Requirement	Check
Certificate of Conformance	☐
SEAKR Part Number / Revision	☐
SEAKR PO Number	☐
Serial Numbers (XXX-YYYY) *XXXX = Panel Number, YYYY = Date Code*	☐
Ionic Certification (prior to solder mask)	☐
Material Certificates	☐
Laminate(s)	☐
Prepreg(s)	☐
Copper Foil	☐
Solder Mask	☐
Marking Ink	☐
PCB Finish (XRF or C of C equivalent)	☐
Coverlay (if applicable)	☐
Via fill (if applicable) *Complies with approved materials in **Section 3.1.8***	☐
Microsection Report	☐
SEAKR Part Number / Revision	☐
Serial Numbers (XXX-YYYY) *XXXX = Panel Number, YYYY = Date Code*	☐
Thermal Stress Parameters *Temperature and Number of Cycles*	☐
Industry Specification and Revision for Inspection *(e.g., IPC-6012E)*	☐
Inspection Results *For each item in **Section 0***	☐
Solderability Test & Acceptance	☐
Dimensional Measurements	☐
Copper Plating Thickness	☐
Etchback	☐
Backdrill Stub Length (as applicable. Include DNC layer)	☐
Dielectric Thickness	☐
Copper Foil Thickness	☐
Plated Layer Thickness	☐
Representative Photo of each Hole Type *Shows both sides of the plated hole and entire length of hole* *Photos are labeled by coupon type and etch condition* *Verification of NO CUT layers on backdrill coupons (where applicable)*	☐

Dimensional Report (CMM or equivalent)	☐
SEAKR Part Number / Revision	☐
Serial Numbers (XXX-YYYY) Inspected *XXXX = Panel Number, YYYY = Date Code*	☐
Drawing PCB Dimensional Requirements	☐
Dimensional Tolerance	☐
Measured Values	☐
Tool Used for Measurement	☐
Visual Inspection Report	☐
SEAKR Part Number / Revision	☐
Serial Numbers (XXX-YYYY) *XXXX = Panel Number, YYYY = Date Code*	☐
Industry Specification and Revision for Inspection *(e.g., IPC-6012E)*	☐
Inspection Criteria Evaluated	☐
Pass / Fail Indication	☐
Statement verifying 100% inspection	☐
Electrical Test Report	☐
SEAKR Part Number / Revision	☐
Serial Numbers (XXX-YYYY) *XXXX = Panel Number, YYYY = Date Code*	☐
Test site location name and address	☐
Quantity of PCBs tested and accepted	☐
Continuity and Isolation Test Values *See **Section 3.7***	☐
Electrical Test Method Used *Indirect not allowed*	☐
Hi-pot certification (if applicable)	☐
Operator Signature and Date	☐
Impedance Test Report	☐
SEAKR Part Number / Revision	☐
Lot Date Code	☐
Panel Numbers Tested	☐
Impedance Test Results for each Panel	☐
Test Structure Name	☐
Target Impedance	☐
Impedance Tolerance	☐
Impedance Measurement	☐
All applicable SEAKR Approved Waivers	☐
All applicable SEAKR Approved Deviation Requests	☐
SEAKR Approved PCB Stack-up	☐